



# UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE  
United States Patent and Trademark Office  
Address: COMMISSIONER FOR PATENTS  
P.O. Box 1450  
Alexandria, Virginia 22313-1450  
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/691,966	10/24/2003	Khader S. Abdel-Hafez	3359-Z	6973
7590 09/08/2004			EXAMINER	
Law Office of Jim Zegeer Suite 108 801 North Pitt Street Alexandria, VA 22314			TRIMMINGS, JOHN P	
			ART UNIT	PAPER NUMBER
			2133	

DATE MAILED: 09/08/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

<p align="center"><b>Office Action Summary</b></p>	<b>Application No.</b> 10/691,966	<b>Applicant(s)</b> ABDEL-HAFEZ ET AL.	
	<b>Examiner</b> John P Trimmings	<b>Art Unit</b> 2133	

**-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --**

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 24 October 2003.
- 2a) ☐ This action is **FINAL**.                      2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-82 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-82 is/are rejected.
- 7) ☒ Claim(s) 18 is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☒ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 24 October 2003 is/are: a) ☐ accepted or b) ☒ objected to by the Examiner.  
 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
 Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All    b) ☐ Some \*    c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- |  |  |
|--|--|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) ✓<br>2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)<br>3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)<br>Paper No(s)/Mail Date _____. | 4) <input type="checkbox"/> Interview Summary (PTO-413)<br>Paper No(s)/Mail Date. _____.<br>5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)<br>6) <input type="checkbox"/> Other: _____. |
|--|--|

### **DETAILED ACTION**

Claims 1-82 are presented for examination.

#### ***Priority***

The examiner acknowledges the applicant's claim of priority of 10/30/2002, based on a provisional application 60/422,117.

#### ***Drawings***

1. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they include the following reference character(s) not mentioned in the description:

FIG.2A,B,C,D,E 204.

FIG.2E 283 & 284.

FIG.3A 313 & 314.

FIG.3B 349 & 350.

FIG.3C 384-387, 373, 374, 391.

FIG.4A 401a & 403a.

FIG.4B 411a & 413a.

FIG.4C 421a & 423a.

FIG.4D 431a & 433a.

FIG.4E 441a, 443a, 444a, 446a.

FIG.4F 451a, 453a, 454a, 456a.

FIG.4G 401b & 403b.

FIG.4H 411b & 413b.

FIG.4I 431b, 433b, 434b, 436b.

FIG.4J 451b, 453b, 454b, 456b.

FIG.5C,D 533 & 534.

FIG.5E,F 564, 569, 570.

Corrected drawing sheets, or amendment to the specification to add the reference character(s) in the description, are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

2. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they do not include the following reference character(s) mentioned in the description:

"design 200" (page 25).

"result 220" (page 26).

"result 240", "result 260" (page 27).

"result 280" (page 28).  
"diagram 300" (page 29).  
"embodiment 370" (page 33).  
"diagram 400a", "diagram 410a" (page 34).  
"diagram 420a" (page 35).  
"diagram 430a", "diagram 440a" (page 36).  
"diagram 450a" (page 37).  
"diagram 400b" (page 38).  
"diagram 410b" (page 39).  
"diagram 430b", "diagram 450b" (page 40).  
"set 500" (page 41).  
"model 560", "model 580" (page 45).  
"diagram 600", "diagram 700" (page 47).  
"diagram 750" (page 48).  
"system 800" (page 49).

Corrected drawing sheets are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the

applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

### ***Claim Objections***

3. Claim 18 is objected to because of the following informalities: the citation, "said enable" in line 3 should read, "said scan enable". Appropriate correction is required.

### ***Specification***

4. The disclosure is objected to because of the following informalities:

Page 11 line 4 recites, "easily adapted" but the examiner believes it should read, "easily be adapted". Appropriate correction is required.

Page 16 lines 5, 9; "repaired" is misspelled.

Page 48 line 21 recites, "code 701" but the examiner believes it should read, "code 751".

5. The abstract of the disclosure is objected to because the narrative is 173 words in length. Correction is required. See MPEP § 608.01(b).

Applicant is reminded of the proper language and format for an abstract of the disclosure. The abstract should be in narrative form and generally limited to a single paragraph on a separate sheet within the range of 50 to 150 words. It is important that the abstract not exceed 150 words in length since the space provided for the abstract on the computer tape used by the printer is limited. The form and legal phraseology often used in patent claims, such as "means" and "said," should be avoided. The abstract should describe the disclosure sufficiently to assist readers in deciding whether there is a need for consulting the full patent text for details.

The language should be clear and concise and should not repeat information given in the title. It should avoid using phrases which can be implied, such as, "The disclosure concerns," "The disclosure defined by this invention," "The disclosure describes," etc.

***Claim Rejections - 35 USC § 112***

The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

6. Claim 9 recites the limitation "said ATE" in line 2. There is insufficient antecedent basis for this limitation in the claim.

***Claim Rejections - 35 USC § 102***

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

7. Claims 1, 3-8, 11, 13, 15 and 16 are rejected under 35 U.S.C. 102(b) as being anticipated by Ahanin et al., U.S. Patent No. 5166604.

As per Claim 1:

Ahanin et al. teaches a method (see Title) for testing faults propagated to the data ports and asynchronous set/reset ports of scan cells in a scan-based integrated circuit in a scan-test mode, the scan-based integrated circuit containing a plurality of set/reset circuitries, and a plurality of scan chains, each scan chain comprising multiple

scan cells coupled in series (column 2 lines 22-52 and Fig.1), each scan cell having one or more clocks (FIG.2 normal and scan clocks) and having a scan enable (SE) signal (FIG.2 12d) and a set/reset enable (SR EN) signal (FIG.2 12h); said method comprising: shifting in a stimulus to all said scan cells in said scan-based integrated circuit by enabling all said scan enable (SE) signals connected to all said scan cells during a shift-in operation (column 3 lines 29-48), capturing a test response of all said scan cells for testing said faults propagated to said data ports and said asynchronous set/reset ports of all said selected scan cells by enabling or disabling all said set/reset enable (SR-EN) signals connected to all said selected scan cells during a capture operation (column 5 lines 1-11); and shifting out said test response for comparison while shifting in new stimulus to all said scan cells during a shift-out operation (column 2 lines 50-52).

As per Claim 3:

Ahanin et al. further teaches the method of claim 1, wherein said shifting in a stimulus to all said scan cells further comprises using all said set/reset enable (SR-EN) signals to disable all said asynchronous set/reset ports of all said selected scan cells during said shift-in operation (column 3 lines 29-34).

As per Claim 4:

Ahanin et al. further teaches the method of claim 1, wherein said capturing a test response of all said scan cells further comprises selectively disabling all said scan enable (SE) signals simultaneously or in an ordered sequence during said capture operation (column 2 lines 46-50).

As per Claim 5:

Ahanin et al. further teaches the method of claim 1, wherein said capturing a test response of all said scan cells further comprises disabling all said clocks controlling all said scan cells, while enabling all said set/reset enable (SR EN) signals, for testing said faults propagated to said asynchronous set/reset ports of all said selected scan cells during said capture operation (column 5 lines 1-11).

As per Claim 6:

Ahanin et al. further teaches the method of claim 5, wherein said enabling all said set/reset enable (SR-EN) signals further comprises selectively enabling two or more (column 5 line 2) said set/reset enable (SR EN) signals during said capture operation (column 4 lines 48-68 and column 5 lines 1-11).

As per Claim 7:

Ahanin et al. further teaches the method of claim 1, wherein said capturing a test response of all said scan cells further comprises enabling all said clocks controlling all said scan cells, while disabling all said set/reset enable (SR EN) signals, for testing said faults propagated to said data ports of all said selected scan cells during said capture operation (column 4 lines 64-68).

As per Claim 8:

Ahanin et al. further teaches the method of claim 7, wherein said enabling all said clocks controlling all said scan cells further comprises selectively enabling two or more said clocks controlling two or more said scan cells simultaneously or in an ordered sequence during said capture operation (FIG.2 12f and column 4 lines 64-68).

As per Claim 11:

Ahanin et al. further teaches the method of claim 1, wherein said scan enable (SE) signal is an input signal to said scan-based integrated circuit (FIG.2 12d).

As per Claim 13:

Ahanin et al. further teaches the method of claim 1, wherein said set/reset enable (SR-EN) signal is an input signal to said scan-based integrated circuit (FIG.2 12h, 12k).

As per Claim 15:

Ahanin et al. further teaches the method of claim 1, wherein said scan cell is a multiplexed-type D flip-flop (FIG.1).

As per Claim 16:

Ahanin et al. further teaches the method of claim 1, wherein said set/reset controller is used to repair one or more asynchronous set/reset violations, comprising sequentially-gated set/reset violations, combinationally-gated set/reset violations, generated set/reset violations, and destructive set/reset violations, in a selected set/reset circuitry in said scan-based integrated circuit (see Abstract and column 1 lines 6-66).

### ***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

8. Claims 2, 9, 12 and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ahanin et al., U.S. Patent No. 5166604.

As per Claims 2 and 9:

Ahanin et al. teaches the method of claim 1, wherein said shifting in a stimulus to all said scan cells (column 3 lines 29-48) further comprises selectively shifting in a predetermined stimulus from an ATE (automatic test equipment) in said selected scan-test mode (FIG.2 12e). Ahanin et al. further teaches the method of claim 1, wherein said shifting out said test response for comparison further comprises selectively shifting out said test response to said ATE for comparison in said selected scan-test (column 2 lines 50-52 and column 5 lines 37-46). It would have been obvious to one with ordinary skill in the art at the time of the invention to recognize terminal 12e of the reference to be a data input from an external source, which in the art would have been an ATE.

As per Claim 12:

Ahanin et al. further teaches the method of claim 11, wherein all said scan enable (SE) signals are further driven by one or more global scan enable (global-SE) signals (column 1 lines 34-666), wherein each said global scan enable (global-SE) signal is an input signal to said scan-based integrated circuit (FIG.2 12d). It would have been obvious to one with ordinary skill in the art at the time of the invention to recognize terminal 12f of the reference to be a scan-enable input from an external source, which in the art would have been considered to be a "global enable" signal, originated from an ATE.

As per Claim 14:

Ahanin et al. further teaches the method of claim 13, wherein all set/reset enable (SR EN) signals are further driven by one or more global set/reset enable (global-SR-EN) signals (FIG.2 12h, 12k, wherein each said global set/reset enable (global-SR-EN) signal is an input signal to said scan-based integrated circuit. It would have been obvious to one with ordinary skill in the art at the time of the invention to recognize terminal 12h and 12k of the reference to be an enable input from an external source, which in the art would have been considered to be a "global enable" signal, originated from an ATE.

9. Claims 10 and 17-30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ahanin et al., U.S. Patent No. 5166604, in view of the applicant's own Prior Art of FIG.2D.

As per Claim 10:

Ahanin et al. teaches the method of claim 1, wherein said set/reset controller further comprises providing a capture controller in response to a said scan enable (SE) signal and a said set/reset enable (SR EN) signal, wherein said shift controller is adapted to disable said asynchronous set/reset ports of one or more said selected scan cells during said shift-in or said shift-out operation (column 3 lines 29-48), and wherein said capture controller is adapted to enable or disable propagation of said faults present in one said set/reset circuitry to said asynchronous set/reset ports of one or more said selected scan cells during said capture operation (column 5 lines 1-11). However, Ahanin et al. does not teach a shift controller for disabling said asynchronous set/reset ports of all scan cells, under control of the scan enable (SE) and set/reset enable (SR-

EN) signal. But the analogous prior art reference in the applicant's disclosure (Background, page 6) and drawing (FIG.2D) provides the teaching of this feature. And, on page 6, the applicant provides for an advantage of the circuit of applicant figure 4D to the effect that the set/reset faults advantageously can be detected during a scan test "capture" cycle. And one with ordinary skill in the art at the time of the invention, motivated by the above, would find it obvious to add the applicant's prior art circuit of FIG.4D with the circuit of Ahanin et al. in order to improve set/reset detection capabilities in a scan circuit.

As per Claim 17:

Ahanin et al. teaches a set/reset controller having a scan enable (SE) signal (FIG.1 12d) and a set/reset enable (SR-EN) signal (FIG.2 12h) for testing faults propagated to the asynchronous set/reset ports of scan cells in a scan-based integrated circuit (FIG.1 20), the scan-based integrated circuit containing a plurality of set/reset circuitries (FIG.2 12h) and a plurality of scan chains (FIG.1 20), each scan chain comprising multiple scan cells coupled in series (FIG.1 20-1 to 20-2), each scan cell having one or more clocks (FIG.2 normal and scan clocks); said set/reset controller comprising: a capture controller, inserted between said selected set/reset circuitry and said asynchronous set/reset ports of all said selected scan cells (FIG.2 NORMAL NPRESET 102), for enabling or disabling propagation of said faults present in said selected set/reset circuitry to said asynchronous set/reset ports of all said selected scan cells (FIG.1 20), in response to said scan enable (SE) signal (FIG.2 12d) and said set/reset enable (SR EN) signal (FIG.2 12h), during a capture operation (column 5 lines

1-11). However, Ahanin et al. does not teach a shift controller inserted between the set/reset circuitry and said asynchronous set/reset ports of all scan cells, for disabling said asynchronous set/reset ports of all scan cells, under control of the scan enable (SE) and set/reset enable (SR-EN) signal. But the analogous prior art reference in the applicant's disclosure (Background, page 6) and drawing (FIG.2D) provides the teaching of this feature. And, on page 6, the applicant provides for an advantage of the circuit of applicant figure 4D to the effect that the set/reset faults advantageously can be detected during a scan test "capture" cycle. And one with ordinary skill in the art at the time of the invention, motivated by the above, would find it obvious to add the applicant's prior art circuit of FIG.4D with the circuit of Ahanin et al. in order to improve set/reset detection capabilities in a scan circuit.

As per Claim 18:

Ahanin et al. further teaches the set/reset controller of claim 17, wherein said shift controller is selectively embedded in all said selected scan cells, and wherein said enable (SE) signal, said set/reset enable (SR-EN) signal can be selectively used to disable all said asynchronous set/reset ports of all said selected scan cells during said shift-in operation (column 3 lines 29-48). And in view of previously outlined motivation, the claim is rejected.

As per Claim 19:

Ahanin et al. further teaches the set/reset controller of claim 17, wherein said capture controller further comprises selectively disabling all said scan enable (SE)

signals simultaneously during said capture operation (column 5 lines 1-11 and applicant's FIG. 2D). And in view of previously outlined motivation, the claim is rejected.

As per Claim 20:

Ahanin et al. further teaches the set/reset controller of claim 17, wherein said capture controller further comprises disabling all said clocks controlling all said scan cells, while enabling all said set/reset enable (SR EN) signals, for testing said faults propagated to said asynchronous set/reset ports of all said selected scan cells during said capture operation (column 5 lines 1-11). And in view of previously outlined motivation, the claim is rejected.

As per Claim 21:

Ahanin et al. further teaches the set/reset controller of claim 20, wherein said enabling all said set/reset enable (SR EN) signals further comprises selectively enabling two or more said set/reset enable (SR EN) signals simultaneously during said capture operation (column 4 lines 64-68). And in view of previously outlined motivation, the claim is rejected.

As per Claim 22:

Ahanin et al. further teaches the set/reset controller of claim 17, wherein said capture controller further comprises enabling all said clocks controlling all said scan cells, while disabling all said set/reset enable (SR EN) signals, for testing said faults propagated to said data ports of all said selected scan cells during said capture operation (column 4 lines 48-63). And in view of previously outlined motivation, the claim is rejected.

As per Claim 23:

Ahanin et al. further teaches the set/reset controller of claim 22, wherein said enabling all said clocks controlling all said scan cells further comprises selectively enabling two or more said clocks controlling two or more said scan cells simultaneously (FIG.2 normal and scan clocks). And in view of previously outlined motivation, the claim is rejected.

As per Claim 24:

Ahanin et al. further teaches the set/reset controller of claim 17, wherein said capture controller is embedded in all said selected scan cells (FIG.1 and applicant's FIG2D). And in view of previously outlined motivation, the claim is rejected.

As per Claim 25:

Ahanin et al. further teaches the set/reset controller of claim 17, wherein said scan enable (SE) signal is an input signal to said scan-based integrated circuit (FIG.2 12d). And in view of previously outlined motivation, the claim is rejected.

As per Claim 26:

Ahanin et al. further teaches the set/reset controller of claim 25, wherein all said scan enable (SE) signals are further driven by one or more global scan enable (global-SE) signals (FIG.2 12d), wherein each said global scan enable (global-SE) signal is an input signal to said scan-based integrated circuit. It would have been obvious to one with ordinary skill in the art at the time of the invention to recognize terminal 12d of the reference to be an enable input from an external source, which in the art would have

Art Unit: 2133

been considered to be a "global enable" signal, originated from an ATE. And in view of previously outlined motivation, the claim is rejected.

As per Claim 27:

Ahanin et al. further teaches the set/reset controller of claim 17, wherein said set/reset enable (SR-EN) signal is an input signal to said scan-based integrated circuit (FIG.2 12h, 12k). And in view of previously outlined motivation, the claim is rejected.

As per Claim 28:

Ahanin et al. further teaches the set/reset controller of claim 27, wherein all set/reset enable (SR EN) signals are further driven by one or more global set/reset enable (global-SR-EN) signals (FIG.2 12h, 12k), wherein each said global set/reset enable (global-SR-EN) signal is an input signal to said scan-based integrated circuit. It would have been obvious to one with ordinary skill in the art at the time of the invention to recognize terminal 12h and 12k of the reference to be an enable input from an external source, which in the art would have been considered to be a "global enable" signal, originated from an ATE. And in view of previously outlined motivation, the claim is rejected.

As per Claim 29:

Ahanin et al. further teaches the set/reset controller of claim 17, wherein said scan cell is a multiplexed-type D flip-flop (see FIG.1). And in view of previously outlined motivation, the claim is rejected.

As per Claim 30:

Ahanin et al. further teaches the set/reset controller of claim 17, wherein said shift controller and capture controller are used to repair one or more asynchronous set/reset violations, comprising sequentially-gated set/reset violations, combinationally-gated set/reset violations, generated set/reset violations, and destructive set/reset violations, in said selected set/reset circuitry in said scan-based integrated circuit (see Abstract and column 1 lines 6-66). And in view of previously outlined motivation, the claim is rejected.

10. Claims 31-82 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ahanin et al., U.S. Patent No. 5166604, in view of the applicant's own prior art of FIG. 2D, and further in view of Ruiz et al., U.S. Patent No. 6195776. The circuit based on the teachings of Ahanin et al. in Claim 1-16 is synthesized into a logic netlist and a test program using an electronic design automation system based on HDL techniques in a computer based program, as is common in the art (see Abstract of Ruiz et al. and FIG.5), and where all of the circuit characteristics of claims 17-30 of the applicant are built in to the simulations and syntheses of the method of Ruiz et al. (see column 5 lines 30-67 and column 6 lines 1-15). And, Ruiz et al., in column 5 lines 11-28 boasts of a better way to build netlists and ATPG programs much faster than the state of the art. One with ordinary skill in the art at the time of the invention, motivated as suggested, would combine the teachings of Ruiz et al. to the scan circuit system requirements of Ahanin et al. in order to improve the efficiency of the overall process of circuit design.

**Conclusion**


Any inquiry concerning this communication or earlier communications from the examiner should be directed to John P Trimmings whose telephone number is 703-305-0714. The examiner can normally be reached on Monday through Thursday, 7:30 AM to 6:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert DeCady can be reached on 703-305-9595. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

  
John P Trimmings  
Examiner  
Art Unit 2133

jpt

  
Guy J. Lamarre  
Primary Examiner